Register No : _____

THE KAVERY ENGINEERING COLLEGE

(An Autonomous Institution)

B.E/B.TECH DEGREE END SEMESTER THEORY EXAMINATIONS, NOV /DEC 2024

Fifth Semester

Electronics and Communication Engineering

EC3552 - VLSI and Chip Design

Regulations - 2021

Duration : 3 Hrs *Maximum : 100 Marks*

*PART – A (ANSWER ALL QUESTIONS) (Marks 10*2=20)*

Q.No	*Questions*	*BLT*	*CO*	*Marks*
1.	Define threshold voltage in MOSFETs.	RE	1	2
2.	Distinguish between ideal and non-ideal IV characteristics in MOSFETs.	UN	1	2
3.	Define Elmore's constant.	RE	2	2
4.	Implement the following logic function using pass transistor logic. Y= (A+B)'	AP	2	2
5.	Compare static latch and dynamic latch.	UN	3	2
6.	What is a setup time in sequential circuits?	RE	3	2
7.	Define interconnect capacitance in VLSI circuits.	RE	4	2
8.	Mention some advantage of using FPGAs over fixed-function digital circuits.	UN	4	2
9.	Define the term "System on Chip".	RE	5	2
10.	What is the role of scan chains in boundary scan design.	UN	5	2

*PART – B (ANSWER ALL QUESTIONS) (Marks 5*13 = 65)*

Q.No			*Questions*	*BLT*	*CO*	*Marks*
11.	a		Describe the equation for source to drain current in the three regions of operation of a MOS transistor and draw the VI characteristics.	UN	1	13
			Or			
	b	i	Explain the dynamic behavior of MOSFET transistor with neat diagram.	UN	1	7
		ii	Describe the factors contributing to power consumption in CMOS circuits.	UN	1	6
12.	a	i	Sketch the stick diagram of 2-input NAND and NOR gate.	AP	2	6
		ii	Design a transmission gate based implementation of 4x1 MUX and XOR gate.	AP	2	7
			Or			
	b	i	Draw the static CMOS logic circuit for the following Boolean functions $Y= \overline{A+B.C}$, $Y= \overline{(A+B).(C+D)}$	AP	2	6
		ii	Apply the low power design principles to a CMOS circuit and explain its effects.	AP	2	7

13.	a	Elucidate the methodology of sequential circuit design of static latches and registers.	UN	3	13
		Or			
	b	Describe the concept of pipelining in digital systems. Explain how pipelines improve device performance.	UN	3	13
14.	a	Design a carry look ahead logic for a 4- bit adder. Justify that carry look ahead adder is faster than ripple carry adder.	AP	4	13
		Or			
	b	Design a booth multiplier to multiply two positive numbers. Justify how booth algorithm speeds up a multiplication process.	AP	4	13
15.	a	Describe the wafer-to-chip fabrication process flow. Explain the key stages from silicon wafer preparation to final chip packaging.	UN	5	13
		Or			
	b	Discuss Automatic Test Pattern Generation (ATPG). Explain its role in the testing process and its impact on the efficiency and accuracy of chip verification.	UN	5	13

*PART – C (Marks 1*15 = 15)*

Q.No		*Questions*	*BLT*	*CO*	*Marks*
16.	a	Apply 90nm technology library design rules to sketch the layout of 3 input NAND and NOR gate.	AP	2	15
		Or			
	b	Implement the following functions using PAL. i) W(A,B,C,D)=Σm(1,3,5,7,8,10,12,13) ii) X(A,B,C,D)=Σm(0,2,6,8,9,14) iii) Y(A,B,C,D)=Σm(0,3,7,9,11,12,14)	AP	4	15